REMARKS

Applicant thanks the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119 and receipt of the certified copy of the priority document.

Applicant thanks the Examiner for considering the Information Disclosure Statement filed on May 25, 2001.

The title of the invention has been objected to. A new title is provided herewith. It is submitted that the new title is sufficiently descriptive and therefore the objection to the title should be withdrawn.

The drawings have been objected in that Figures 1-3 were not labeled "prior art". Corrected drawings are submitted herewith by which Figures 1-3 are labeled "prior art". Therefore the objection to the drawings should be withdrawn.

Claims 1-22 had been presented for examination. Claims 1-8 and 10-13 have been withdrawn from consideration based upon the Examiner's restriction/election requirement. Claims 9 and 14-22 have been rejected variously under 35 U.S.C. § 112 (second paragraph) and 35 U.S.C. § 102(e). While these rejections are respectfully traversed, applicant cancels claims 1-22 without disclaimer or prejudice to the filing of continuing applications in this matter. New claims 23-30 are submitted herewith.

It is respectfully submitted that independent claim 23 and its dependent claims 24-30 patentably distinguish over the prior art.

Specifically, the present invention relates to a method of manufacturing a semiconductor memory device having a source area formed by a self-aligned process. According to the semiconductor memory device of the present invention, two memory cells have source areas on a

semiconductor substrate which are commonly connected to each other between two of the word lines, and those pair of memory cells are arranged in a direction, in which word lines are elongated. Those source areas are formed by removing an isolation insulating film and tunnel insulating films at a region sandwiched between two of the word lines. In the process for removing them, because the thickness of the isolation insulating film and the thickness of the tunnel insulating films are different from each other, the isolation insulating films are removed by digging the semiconductor substrate deeply and the tunnel insulating films are removed by digging the semiconductor substrate shallowly to form the source area having an uneven surface. When a silicide layer is formed on the uneven surface of the source area, a completed silicide layer has many disconnections as explained in the specification of the present invention (page 4, lines 1-8 and FIG. 3E).

As a result, a resistance value of the source area is often about 10 times larger than a design resistance value which is estimated without disconnections. This causes a problem with the memory device. Further, in the memory device having a memory cell in a matrix, each source area, which is connected in the semiconductor substrate as a diffusion layer in a direction of the elongated word line, has a different resistance value from each other, which causes a problem as well.

A problem to be solved by the present invention is to provide a memory cell, whose resistance of the source area is provided as a design value, although the source area has an uneven surface. According to the present invention, the source area is covered by a mask during the self-aligned silicide process.

On the other hand, Nomachi et al. deals with a different device from the present invention, end does not teach or suggest the problem to be solved by the present invention at all. Nomachi et al. relates to a so-called trench DRAM having the gates 16a and l6b being elongated in a perpendicular direction to the paper. A plurality of openings of element separating region 14 are elongated in a direction from the gate 16a to the gate 16b and are arranged between those gates 16a, 16b in said perpendicular direction In those openings, N-type diffusion layers 20 as indicated in cross sectional views FIGS. 1-15 are formed. The element separating region 14 is kept remaining at a region surrounded by the gates 16a and 16b and two of the openings of the element separating region 14. Therefore, N-type diffusion layers 20 are independent from each other by separating with the element separating region 14 at a region between two of the gates 16a and 16b. That means that the region sandwiched between the gates 16a and 16b does not have an uneven surface of a semiconductor substrate. As explained above, the device disclosed in Nomachi et al. does not have the problem to be solved by the present invention.

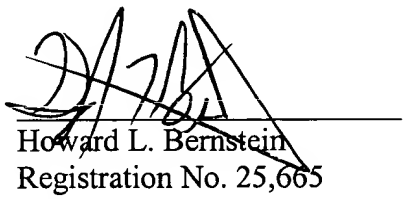
The Examiner pointed out that a silicidation blocking layer 21 is formed on a surface of the second source area, as shown in FIG. 13 of Nomachi et al. However, the insulating film 21 is not formed on any source area having an uneven surface. It is formed only on the plane source area which is surrounded by the gates 16a and 16b and the element separating region 14 for preventing a leakage current through the PN junction consisting of the silicon substrate 11 and the N-type diffusion layer 20, as explained in column 2, lines 16-24. Therefore, Nomachi et al. does have a different problem to be solved from the present invention.

Further, Nomachi et al. does not suggest or teach the feature of the present invention, which is the process of removing the isolation insulating film and the tunnel insulating film to form a source area having an uneven surface, or the process of forming a mask on the source area having said uneven surface. Therefore, the present invention is not anticipated or suggested by Nomachi et al.

In view of the foregoing it is respectfully submitted that claims 23-30 are in condition for allowance and that this application should be passed to issue at the earliest possible time. If for any reason the Examiner finds the application other than in condition for allowance he is respectfully requested to call the undersigned attorney at the Washington, D.C. telephone number 293-7060 to discuss the steps necessary for placing the application in condition for allowance.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title is changed as follows:

SEMICONDUCTOR DEVICE HAVING A MEMORY CELL REGION AND A PERIPHERAL CIRCUIT REGION AND METHOD OF MANUFACTURING THEREOF

IN THE CLAIMS:

Claims 1-22 are canceled without prejudice or disclaimer.

Claims 23-30 are added as new claims.